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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,154	11/03/2000	Marlo Nemirovsky	P3816	5008

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	3

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,154	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2002 and 03 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *1,3,5-7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-12 have been examined.

Papers Received

2. Receipt is acknowledged of Information Disclosure Statement papers submitted, where the papers have been placed of record in the file.

Specification

3. The disclosure is objected to because of the following informalities:

- The headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c).
- On page 5, line 16, the word "and" is consecutively repeated.

Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

5. The drawings are objected to because in Figure 3 the number of bits for the connection between elements 35 and 37 are not shown even though there exists a slash through the connection such as is well known in the art to be used in conjunction with a number to indicate the bus width. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 1 is objected to because of the following informalities:

- Line 13 has a semicolon at its end. This semicolon should not be here if it is intended that the next paragraph speaking of a characterization be describing the select system because the semicolon is in effect separating the paragraph from every other paragraph of the claim in subject matter. The examiner is taking the intent of the applicant to be for the characterization description to be of the select system.
- The last paragraph of the claim says that the number of streams selected for which to fetch instructions is fewer than the number of streams in the plurality of streams. In line 5, it is stated that there exist a plurality of streams fetching instructions. These two statements are inconsistent because one shows that all streams are fetching and one says that a number fewer than the total are fetching. The examiner is taking the phrase that describes a portion of the total number of streams are fetching instructions to be the correct statement based upon the specification. The examiner is subsequently taking the other statement to mean, "a plurality of streams that can be used for fetching instructions from the instruction source."

7. Claims 3 and 9 are objected to because of the following informalities: The both contain the phrase, "directs fetching if instructions beginning at addresses according to the to the program counters," which is unclear. The examiner is taking the phrase to mean, "directs fetching of instructions beginning at addresses according to the program counters."

8. Claim 5 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim states that which was already specifically claimed in claim 1.

9. Claim 6 is objected to because of the following informalities: The claim refers to Arithmetic-Logic Units as begin abbreviated "ALU" when in claim 12 and the specification the abbreviation "ALS" is used. The examiner asks that consistent notation be used.

10. Claim 7 is objected to because of the following informalities:

- Indent (a) mentions a set of instruction queues when "an instruction queue" has already been defined. It is unclear if these queues are replacing the previously mentioned one or if it is a separate entity. The examiner is taking the mentioned "an instruction queue" to mean "an instruction source" in order to remain consistent with claim 1 and the specification. This interpretation also extends to "the instruction queue" mentioned in indent (a) so that it means "the instruction source."
- The preamble says, "a method for decoupling fetching from a dispatch stage." This phrase is unclear as is the meaning of word decoupling in this context . The examiner is taking the phrase to try and point out that each thread is storing instructions in a separate queue before the dispatch stage.

11. Claims 11 and 12 are objected to because of the following informalities: The claims give a parent claim as the method of claim 6 but that claim is an apparatus, not a method. The examiner is taking claim 11 to be referring back to the processor of claim 6 rather than the method and claim 12 to be referring to the processor of claim 11 rather than the method.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 4 recites the limitation "the instruction cache" in line 28. There is insufficient antecedent basis for this limitation in the claim. There is no mention of an instruction cache in claims 1 or 2. The examiner is taking the phrase to mean "an instruction source" based on support for a cache in the specification.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Emer (6,470,443 B1).

17. In regard to claim 1, Emer discloses a pipelined multistreaming processor, comprising:

a. an instruction source; Emer discloses a main memory (figure 1, element 14) and/or an instruction cache (figure 2, element 24) that is used to store the instruction stream as stated in column 3, lines 44-46.

b. a plurality of streams fetching instructions from the instruction source; Emer discloses in Figure 2, how the multiple streams (threads) indicated by each program counter (element 22) fetch instructions using a fetch unit (element 20) in conjunction with the instruction source mentioned above.

c. a dispatch stage for selecting and dispatching instructions to a set of execution units; In column 5, lines 1-3, Emer discloses that as operands for each instruction become available, the instructions are issued out-of order to the appropriate functional unit as shown in Figure 2. It is well known to one of ordinary skill in the art that issuing has the same effect as dispatching in that operands are sent to appropriate execution units.

d. a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage; In column 6, lines 24-27, Emer teaches that instructions can be fetched and then stored in a buffer (queue). In column 4, lines 8-9, Emer discloses an embodiment of his invention where a distinct fetch

unit is included for each thread (stream). Therefore there exists a queue for each fetch unit and thus one queue for each stream. These queues are located after the instruction source since they are after the fetching unit, which gets instructions from the source. The queues are also before the dispatch stage discussed above that sends operands to the functional units.

e. a select system (figure 4, element 62) for selecting streams (elements 22a-22h) in each cycle to fetch instructions from the source (element 24);

f. characterized in that the number of streams selected (figure 4, fetch address) for which to fetch instructions in each cycle (column 4, line 6) is fewer than the number of streams in the plurality of streams (elements 22a-22h). Figure 4 shows how there are multiple streams to be selected from and that one (the fetch address) is selected each cycle. This one is less than the whole of the eight streams presented.

18. In regard to claim 2, Emer discloses the processor of claim 1 wherein the number of streams in the plurality of streams is eight (column 3, lines 63-64), and the number of streams selected for which to fetch instructions in each cycle (column 4, line 6) is two (column 4, lines 3-4, at least one). The range disclosed by Emer of at least one includes the applicant's desired number of streams, two.

19. In regard to claim 3, Emer discloses the processor of claim 2 wherein the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream (column 3, lines 63-64), and directs fetching of instructions beginning at addresses according to the program counters (column 4, lines 2-6).

20. In regard to claim 4, Emer discloses the processor of claim 2 wherein each stream selected to fetch is directed to fetch eight instructions from an instruction cache (column 4, lines 1-6).

21. In regard to claim 5, Emer discloses all of the matter in claim 5 as discussed in paragraph 17.c above.

22. In regard to claim 6, Emer discloses the processor of claim 5 wherein the set of execution units comprises eight Arithmetic-Logic Units (ALUs), and two memory units. It is well known to one of ordinary skill that an execution unit is inherently known as a functional unit. Therefore, each of the ALUs and memory units are functional units. The indication by Emer of multiple functional units (figure 2, element 34) includes the limitation of these ten functional units disclosed in the claim.

23. In regard to claim 7, Emer discloses in a pipelined multistreaming processor (figure 2) having an instruction source (figure 2, element 40 or figure 1, element 14), a method for decoupling fetching from a dispatch stage, comprising the steps of:

a. Placing a set of instruction queues, one for each stream, in the pipeline between the instruction source and the dispatch stage; In column 6, lines 24-27, Emer teaches that instructions can be fetched and then stored in a buffer (queue). In column 4, lines 8-9, Emer discloses an embodiment of his invention where a distinct fetch unit is included for each thread (stream). Therefore there exists a queue for each fetch unit and thus one queue for each stream. These queues are located after the instruction source since they are after the fetching

unit, which gets instructions from the source. The queues are also before the dispatch stage discussed above that sends operands to the functional units.

b. Selecting (figure 4, element 62) one or more streams (figure 4, fetch address), fewer than the number of streams (elements 22a-22h) in the multistreaming processor, for which to fetch instructions in each cycle from an instruction source. Emer discloses in Figure 2, how the multiple streams (threads) indicated by each program counter (element 22) fetch instructions using a fetch unit (element 20).

24. In regard to claim 8, Emer discloses the method of claim 7 wherein the number of streams in the plurality of streams is eight (column 3, lines 63-64), and the number of streams selected for which to fetch instructions in each cycle (column 4, line 6) is two (column 4, lines 3-4, at least one).

25. In regard to claim 9, Emer discloses the method of claim 8 wherein the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream (column 3, lines 63-64), and directs fetching of instructions beginning at addresses according to the program counters (column 4, lines 3-6).

26. In regard to claim 10, Emer discloses the method claim 7 wherein each stream selected to fetch is directed to fetch eight instructions from an instruction source (column 4, lines 1-6).

27. In regard to claim 11, Emer discloses the method of claim 6 wherein the dispatch stage dispatches instructions to a set of execution units. In column 5, lines 1-3, Emer discloses that as operands for each instruction become available, the instructions are

issued out-of order to the appropriate functional unit (execution unit) as shown in Figure 2. It is well known to one of ordinary skill in the art that issuing has the same effect as dispatching in that operands are sent to appropriate execution units.

28. In regard to claim 12, Emer discloses the method of claim 11 wherein the set of execution units comprises eight Arithmetic-Logic Units (ALS), and two memory ports. It is well known to one of ordinary skill that an execution unit is inherently known as a functional unit. Therefore, each of the ALUs and memory ports are functional units. The indication by Emer of multiple functional units (figure 2, element 34) includes the limitation of these ten functional units disclosed in the claim.

Conclusion

29. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited and the references of the PCT or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to multistream selection and instruction queues.

US Pat No 5,430,851 to Hirata shows the use of multiple instruction streams and program counters with a separate fetching means for each stream.

US Pat No 5,574,939 to Keckler shows a multithreaded processor with instruction queue and a prefetch buffer for each thread.

US Pat No 5,742,782 to Ito shows a processor that executes multiple threads in parallel with thread select logic

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
September 10, 2003

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